AMENDMENTS TO THE CLAIMS

Claims 1. – 59. (canceled)

60. (original) A method of forming a resistance variable memory element comprising the steps of:

forming a first electrode;

forming a first chalcogenide glass layer in contact with said first electrode;

forming a first metal containing layer in contact with said first chalcogenide glass layer; and

forming a second chalcogenide glass layer in electrical communication with said first metal containing layer;

forming a second metal containing layer in contact with said first chalcogenide glass layer;

forming a third chalcogenide glass layer in contact with said second metal containing layer; and

forming a second electrode in electrical communication with said third chalcogenide glass layer, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a positive voltage in a first voltage range and from a lower to higher resistance state upon application of a positive voltage in an second voltage range.

61. (original) The method of claim 60 wherein said chalcogenide glass layers comprise a material having the formula Ge_xSe_{100-x}, wherein x is between about 18 to about 43.

62. (original) The method of claim 61 wherein said chalcogenide glass layers have a stoichiometry of about $Ge_{40}Se_{60}$.

63. (original) The method of claim 60 wherein said chalcogenide glass layers comprise a plurality of chalcogenide glass layers.

64. (original) The method of claim 60 wherein said metal containing layers comprise a plurality of metal containing layers.

65. (original) The method of claim 60 wherein one or more of said chalcogenide glass layers contain a metal dopant.

66. (original) The method of claim 60 wherein one or more of said metal containing layers comprises silver-selenide.

67. (original) The method of claim 66 wherein said metal dopant comprises silver.

68. (original) The method of claim 60 wherein said metal containing layers have a thickness which is equal to or greater than the thickness of each of said chalcogenide glass layers.

69. (original) The method of claim 60 wherein each of said metal containing layers has a first thickness and each of said chalcogenide glass layers has a second thickness whereby a thickness ratio of said first thickness to said second thickness is between about 5:1 to about 1:1.

70. (original) The method of claim 69 further wherein said thickness ratio of said first thickness to said second thickness is between about 3.3:1 to about 2:1.

71. (original) A method of forming a resistance variable memory element comprising:

forming a first chalcogenide glass layer;

forming a silver-selenide layer in contact with said first glass layer; and

forming a second chalcogenide glass layer in contact with said silver-selenide layer, said memory element being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of a first positive voltage and from a lower to higher resistance state upon application of a positive voltage in an second voltage.

72. (original) The method of claim 71 wherein said chalcogenide glass material has a stoichiometric composition of about $Ge_{40}Se_{60}$.

73. (original) The method of claim 71 wherein at least one of said glass layers contains a metal dopant.

74. (original) The method of claim 73 wherein said metal dopant comprises silver.

75. (original) The method of claim 71 further comprising the step of forming alternating layers of said chalcogenide glass material and said silver-selenide layer.

76. (original) The method of claim 71 wherein said layer formed of said chalcogenide glass material further contains a metal dopant.

77. (original) The method of claim 76 wherein said metal dopant comprises silver.

78. (original) The method of claim 71 wherein said metal containing layer has a thickness which is equal to or greater than a thickness of each of said first and second chalcogenide glass layers.

79. (original) The method of claim 71 wherein said metal containing layer comprises a plurality of silver-selenide layers in serial contact with each other.

Claims 80. – 101. (canceled)

102. (original) A method of forming a resistance variable memory element comprising:

forming a first electrode;

forming a second electrode; and

forming a plurality of chalcogenide glass layers and at least one metal containing layer between said first and second electrodes, whereby said plurality of chalcogenide glass layers alternate with said at least one metal containing layers, with one of said chalcogenide glass layers being in contact with said first electrode and another of said chalcogenide glass layers being in contact with said second electrode, said layers being constructed and arranged such that a resistance value of said memory element switches from a higher to lower resistance state upon application of first a positive voltage and from a lower to higher resistance state upon application of a second positive voltage.

103. (original) The method of claim 102 wherein said at least one metal containing layers comprises one or more silver-selenide layers.

104. (original) The method of claim 102 wherein one or more of said plurality of chalcogenide glass layers comprises a plurality of chalcogenide glass layers.

105. (original) The method of claim 102 wherein one or more of said at least one metal containing layers comprises a plurality of metal containing layers.

106. (original) The method of claim 102 wherein one or more of said plurality of chalcogenide glass layers contains a metal dopant.

107. (original) The method of claim 106 wherein said metal dopant comprises silver.

Claims 108. – 116. (canceled)